In the claims:

1. (Currently Amended) A device, comprising:

a delay lock loop circuit responsive to an input signal to delay the input signal by a first period and to generate an analog control signal having an amplitude; ~~and~~

a delay circuit coupled to the delay lock loop circuit and responsive to the input signal, the delay circuit being responsive to the analog control signal from the delay lock loop circuit to delay the input signal by a second period as a function of the analog control signal amplitude, the input signal comprising a first clock signal and a second clock signal; and

a circuit coupled to the delay lock loop circuit and the delay circuit, the circuit being operable to receive (a) a data signal, (b) a first delayed clock signal from the delay lock loop circuit, and (c) a second delayed clock signal from the delay circuit to process the data signal.

2. (Previously Amended) A device, comprising:

a delay lock loop circuit responsive to an input signal to delay the input signal by a first period and to generate an analog control signal having an amplitude; and

a delay circuit coupled to the delay lock loop circuit and responsive to the input signal, the delay circuit being responsive to the analog control signal from the delay lock loop circuit to delay the input signal by a second period as a function of the analog control signal amplitude, wherein the input signal comprises complimentary input clock signals.

3. (Original) The device of claim 2, wherein the first period and the second period are substantially the same.

4. (Original) The device of claim 2 further comprising a first input channel coupled to the delay lock loop circuit and a second input channel coupled to the delay circuit.

5. (Previously Amended) The device of claim 2, wherein the delay lock loop circuit further comprises:

at least one delay cell; and

a phase detector responsive to the input signal and responsive to an output signal from the at least one delay cell to produce a control signal.

6. (Previously Amended) The device of claim 2, wherein the delay circuit further comprises at least one delay cell responsive to the control signal from the delay lock loop circuit.

7. (Previously Amended) The device of claim 2, further comprising;

a latch circuit having a first input to receive an input data signal and a second input to receive one of an output from the delay circuit and an output from the delay lock loop circuit.

8. (Original) The device of claim 7, wherein the delay lock loop circuit comprises a center tap.

9. (Currently Amended) A device, comprising:

a delay lock loop circuit responsive to a first clock signal of an input signal to delay the first clock signal by a first period and to generate an analog control signal having an amplitude; ~~and~~

a delay circuit coupled to the delay lock loop circuit and responsive to a second clock signal of the input signal, the delay circuit being responsive to the analog control signal from the delay lock loop circuit to delay the second clock signal by a second period as a function of the analog control signal amplitude; and

a circuit coupled to the delay lock loop circuit and the delay circuit, the circuit being operable to receive (a) a data signal, (b) a first delayed clock signal from the delay lock loop circuit, and (c) a second delayed clock signal from the delay circuit to process the data signal.

10. (Previously Amended) A device, comprising:

a delay lock loop circuit responsive to a first input signal to delay the first input signal by a first period and to generate an analog control signal having an amplitude; and

a delay circuit coupled to the delay lock loop circuit and responsive to a second input signal, the delay circuit being responsive to the analog control signal from the delay lock loop circuit to delay the second signal by a second period as a function of the analog control signal amplitude, wherein the first signal and the second signal comprise complimentary clock signals.

11. (Currently Amended) The device of claim 10 further comprising a latch circuit, the latch being responsive to at

least one of an output of the delay lock loop circuit and an output of the delay circuit.

12. (Previously Amended) The device of claim 10 wherein the delay lock loop circuit comprises at least one delay cell.

13. (Original) The device of claim 11, wherein the delay circuit further comprises at least one delay cell responsive to the control signal from the delay lock loop circuit.

C3

14. (Currently Amended) A method, comprising:

receiving an input signal comprising a first clock signal and a second clock signal;

using a delay lock loop circuit to delay the first clock signal by a first period;

controlling the first period as a function of an analog control signal having an amplitude; ~~and~~

using a delay circuit to delay the second clock signal by a second period in response to the analog control signal amplitude from the delay lock loop circuit; and

receiving (a) a data signal, (b) a first delayed clock signal from the delay lock loop circuit, and (c) a second delayed clock signal from the delay circuit to process the data signal.

15. (Currently Amended) A method, comprising:

receiving an input signal comprising a first clock signal and a second clock signal;

using a delay lock loop circuit to delay the first clock signal by a first period;

controlling the first period as a function of an analog control signal having an amplitude;

using a delay circuit to delay the second clock signal by a second period in response to the analog control signal amplitude from the delay lock loop circuit;

~~The method of claim 16,~~ wherein the using the delay lock loop circuit comprises configuring the delay lock loop circuit with at least one delay cell.

16. (Previously Amended) A method, comprising:

receiving a first signal and a second signal;

using a delay lock loop circuit to delay the first signal by a first period;

controlling the first period as a function of an analog control signal having an amplitude;

using a delay circuit to delay the second signal by a second period in response to the analog control signal amplitude from the delay lock loop circuit; and

activating a latch circuit in response to at least one of an output from the delay lock loop circuit and an output from the delay circuit.

17. (Previously Amended) The method of claim 16, wherein the receiving the first signal and the second signal further comprises receiving a first clock signal and a second clock signal.

18. (Previously Amended) The method of claim 16, wherein the receiving the first signal and the second signal further comprises receiving a first clock signal and a second clock signal and the method further comprising activating a latch

circuit on a rising edge of one of the first delayed clock signal and the second delayed clock signal.

19. (Previously Amended) The method of claim 16, wherein the first period and the second period are substantially the same.

C3

20. (Previously Amended) The method of claim 16, wherein the using the delay circuit further comprises configuring the delay circuit with at least one delay cell and using the control signal to adjust the at least one delay cell.